CMOS chip planarization by chemical mechanical polishing for a vertically stacked metal MEMS integration

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Abstract

In this paper we present the planarization process of a CMOS chip for the integration of a microelectromechanical systems (MEMS) metal mirror array. The CMOS chip, which comes from a commercial foundry, has a bumpy passivation layer due to an underlying aluminum interconnect pattern (1.8 μm high), which is used for addressing individual micromirror array elements. To overcome the tendency for tilt error in the CMOS chip planarization, the approach is to sputter a thick layer of silicon nitride at low temperature and to surround the CMOS chip with dummy silicon pieces that define a polishing plane. The dummy pieces are first lapped down to the height of the CMOS chip, and then all pieces are polished. This process produced a chip surface with a root-mean-square flatness error of less than 100 nm, including tilt and curvature errors.

1. Introduction

Microelectromechanical systems (MEMS) structures and their controlling electronic circuits are commonly interfaced through wire bond connections. By eliminating wire bond connections, MEMS integration on a chip promises advantages such as fast response, small space, low cost packaging, digitized signal processing and high reliability. However, on-chip integration poses a system-level design challenge since the commercial foundry processes of silicon MEMS are generally incompatible with prefabricated CMOS electronics. Specifically, a polysilicon MEMS device is typically post-annealed above 900 °C to reduce residual stress from previous deposition processes [1]. However, aluminum interconnections of CMOS rapidly degrade above 450 °C [2].

Several integration techniques roughly classified as 'CMOS-first' or 'MEMS-first' have been proposed. For the CMOS-first approach, MEMS structures are fabricated during CMOS processing. Tungsten (melting point of 3410 °C) has been suggested as an interconnection metal [8, 9] or

direct polysilicon interconnection [10]. Electroplating can be used to make a MEMS structure on a CMOS wafer [7]. Also, germanium has been introduced as a MEMS structure material [11]. The MEMS structure can be released by reactive ion etching [3, 4] or wet etching using KOH [5] or ethylenediamine-pyrocatechol (EDP) [6]. The MEMS-first approach embeds the MEMS structure in the etched deep trench [12] or forms it with selective epitaxial layers [13] to be followed by the standard CMOS process. A MEMS-first process without a planarization step is also suggested [14]. Alternatives to on-chip integration and wire bonding are chip-packaging techniques such as a gold-plated cable, card-like structure and multi-chip module [15, 16].

In our case, the production of a micro spatial light modulator (μSLM) with 1024 × 1024 pixels motivates the development of methods for on-chip integration. SLMs are used for laser communication and optical correlation applications [17]. To control large numbers of pixels, it is necessary to address the pixels through direct interconnection, rather than off-chip addressing through wire bond connections.
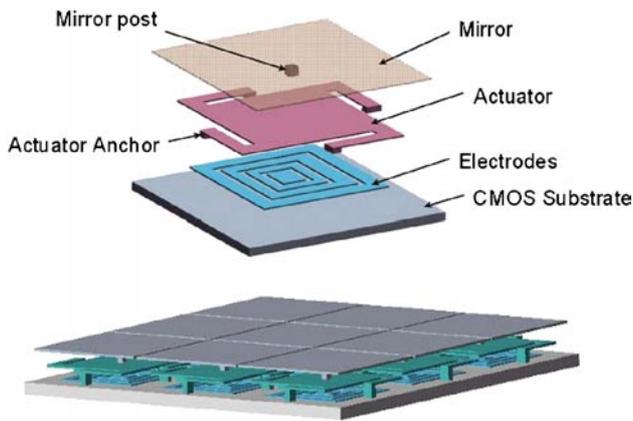
Figure 1. Metal MEMS configuration on a CMOS chip.

Aluminum is proposed for the MEMS structure because it can be deposited at relatively low temperatures (below the CMOS degradation temperature of 450 °C). Metal micromachining has proven successful in the past for the production of large micromirror arrays, most notably for the Texas Instruments Digital Light Processor® [18].

The CMOS chip comes from a commercial foundry and has a bumpy passivation layer due to an underlying aluminum interconnect pattern (1.8 μm high), which is used for addressing individual micromirror array elements. Planarization of the CMOS surface is necessary before fabricating a MEMS structure on top of it. One strategy for planarizing a CMOS chip or wafer is the spinning of benzocyclobutene (BCB) with a low hard cure temperature of 200–250 °C. A multilayer structure of $SiO_2/BCB/SiO_2$ produced a planarization error of 5% but left an edge bead that required subsequent removal [19]. Another BCB application reduced the surface topography from 2.8 μm to about 60 nm [20]. Recently, chemical mechanical polishing (CMP) has played a key role in allowing continued improvements in integrated circuit density, especially metal interconnection technology [21]. It has mostly been used for interlayer dielectric and metal damascene planarization. Also, CMP technology has been successfully used to make multilevel polysilicon MEMS structures [22, 23].

This MEMS μSLM development project makes use of CMOS in die form to confirm the functional requirements before expensive wafer scale integration. In this study we adopt a novel CMP technique for chip planarization.

2. Large-scale spatial light modulator

2.1. Description of micromirror array

A large array of electrostatically actuated, piston-motion MEMS mirrors is to be used as a μSLM for an adaptive optics application [17]. Figure 1 illustrates a nine-mirror segment of the μSLM. The full array consists of 1024 aluminum mirror segments fabricated over a CMOS chip. Each pixel is capable of altering the phase of the light by up to one wavelength infrared light ($\lambda = 1.5$ μm). The underlying CMOS driver provides a resolution of 50 nm over 750 nm of stroke. Mirror elements must be optically flat and more

(*a*)

(*b*)
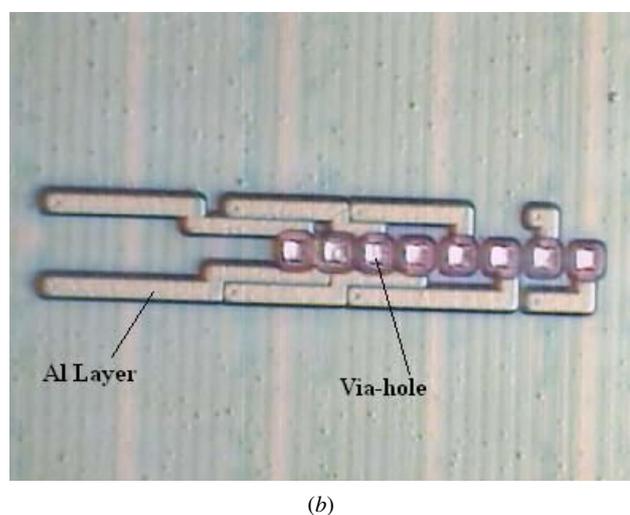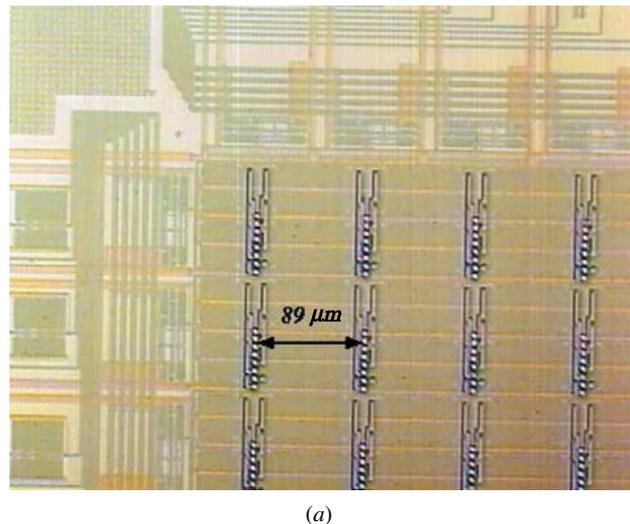
Figure 2. Micrographs of CMOS-1 showing (*a*) interconnect arrangement and (*b*) multiple bit via-holes.

than 90% reflective. The pixels are designed to have a step response time of 10 μs. This design achieves a mirror fill factor of 98%. Because the device is integrated directly with the underlying electronics, it is scalable to mega-pixel array sizes. The significant challenges associated with manufacturing the μSLM are: (1) integration of the MEMS array with the CMOS electronic driver array; (2) production of optical-quality mirror elements using a metal–polymer micromachining process.

2.2. CMOS chip topography

The micromachining process for a prototypical integrated 32 × 32 μSLM array is being developed using foundry-produced CMOS chips. Two types of chips were designed and produced. The first (labeled CMOS-1) is 4 × 4 mm^2 in size while the second (CMOS-2) is 5.5 × 5.5 mm^2. Both have a 32 × 32 array of interconnects for integrating the mirror array on the top of the chips. Figure 2(*a*) shows a corner of a CMOS-1 chip as-received. In the foundry the top passivation layer was etched down to the aluminum layer to form vias as shown in figure 2(*b*).
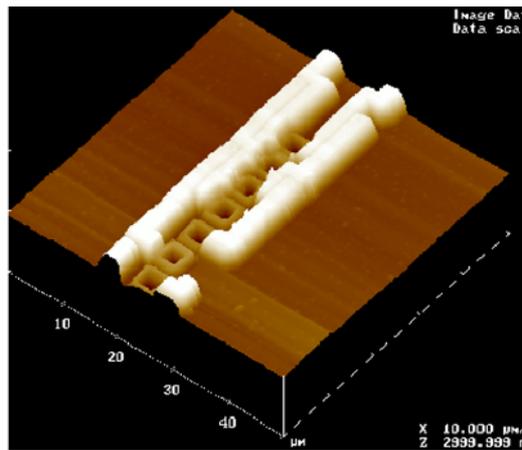
(a)
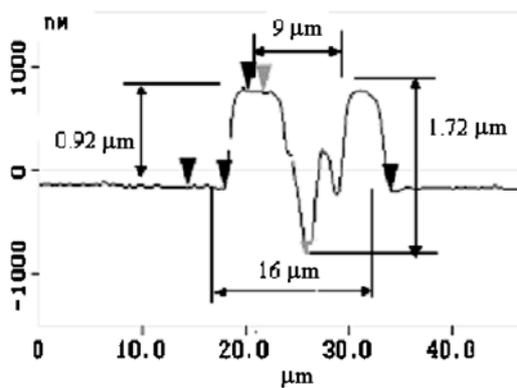
(b)

Figure 3. AFM measurement of the bumps in CMOS-1: (a) 3D image; (b) section profile.

(a)

(b)

Figure 4. Schematic diagrams of CMOS-2: (a) top view of chip; (b) top view of one pixel.

The topography of the CMOS-1 chip around via-holes was investigated. Figure 3(a) shows a three-dimensional (3D) image using atomic force microscopy (AFM). Conformal deposition to cover the underlying aluminum pattern results in bumps of 0.92 μm (equivalent to the aluminum layer thickness; see figure 3(b)). The passivation structure of this CMOS chip (approximated in the figure as 1.72 μm thick) consists of a silicon dioxide layer on the bottom, which is about half of the total thickness, and a silicon nitride layer on top. The bumps are to be removed through the planarization process.

The CMOS-2 chip, shown in figure 4, has bumps 1.8 μm high and four vias per pixel.

3. Low-temperature deposition by sputtering

3.1. Temperature characteristic

The thickness of the passivation layer leaves little room for tilt error during the planarization process. Therefore, additional deposition of either silicon nitride or silicon dioxide was considered. Low-temperature deposition is required to avoid damage to the metallic CMOS circuitry. Both silicon dioxide and silicon nitride have been deposited as interlayer dielectric materials at relatively low temperature using plasma enhanced chemical vapor deposition (PECVD)[24]. Silicon

dioxide mostly functions as an electrical insulating layer while silicon nitride provides environmental protection from sodium ions. Our study pursued another deposition technique, radio-frequency (rf) sputtering. First, the temperature characteristic for the rf sputtering of the two materials was measured. Sputtering was performed at a power setting of 351 W, an argon flow rate of 75 sccm, and an initial vacuum pressure of 6.6×10^{-5} Pa. After pre-sputtering for a few minutes to obtain a stable plasma state, the sputtering temperature was recorded using a temperature gage inside the vacuum chamber. Figure 5 shows how the temperature changes with time for the two materials.

The nominal room temperature was 21 °C, and pre-sputtering for 2 min increased the chamber temperature to 26 °C for silicon dioxide and 23 °C for silicon nitride. In about 60 min, temperatures reached about 90% of their final equilibrium values. The final silicon dioxide and silicon nitride temperatures are 156 °C and 75 °C, respectively. All tests showed no more than a 10% variation in the results. These findings ensure that sputtering temperatures will remain well below the aluminum degradation temperature of 450 °C.
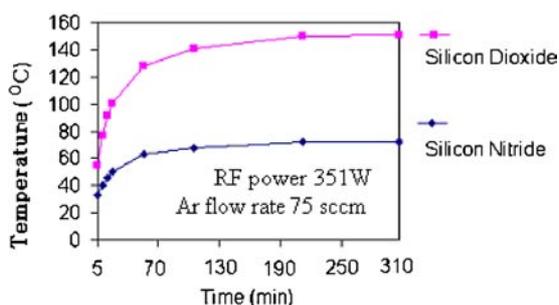
Figure 5. Temperature characteristic for RF sputtering of two passivation materials.
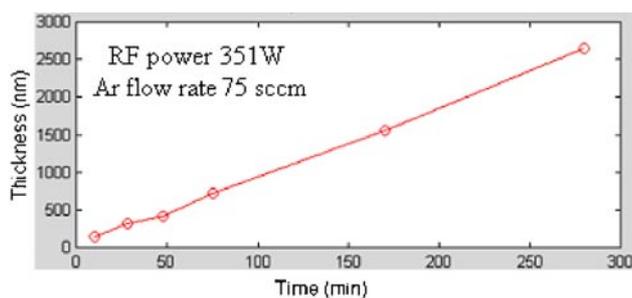
Figure 6. Sputter thickness of silicon nitride with time.

3.2. Sputtering rate

The sputter rate of the two materials was measured while sputtering with the same power and flow rate as above. Figure 6 presents the thickness of silicon nitride after six different sputtering times. Initial chamber pressures for the six tests ranged between 1.3×10^{-5} Pa and 4.2×10^{-5} Pa. For 28 and 280 min, the sputter rates were 11.4 and 9.1 nm min^{-1}, respectively. The sputter rate tends to decrease with time but stabilizes after 170 min (1.56 μm thickness). An additional test of 450 min duration showed a sputter rate of 9.3 nm min^{-1}. Similar tests with silicon dioxide yielded an average sputter rate of 13.4 nm min^{-1}.

The top passivation layer of the as-shipped CMOS is silicon nitride. The deposition of a silicon dioxide layer on top of the bumpy CMOS was considered, but it would create a structure with intermediate planes consisting of both silicon nitride and silicon dioxide. Because the two materials polish at dissimilar rates, a flat surface would be difficult to achieve. Therefore, silicon nitride was chosen as the sputtering material for planarization.

4. Chemical mechanical polishing

4.1. Configuration of polishing machine

Lapping and polishing were performed using a conventional polishing machine with pneumatic pressure and automatic drip slurry. Figure 7 shows a schematic diagram of the lapping and polishing setup. The CMOS chip is bonded to a glass plate. Eight 'dummy' 10×10 mm^2 silicon pieces are bonded with wax around the outer edge of the glass plate. These pieces are initially slightly thicker than the CMOS chip. The lapping plate (with or without a polishing pad on top) is fixed to a
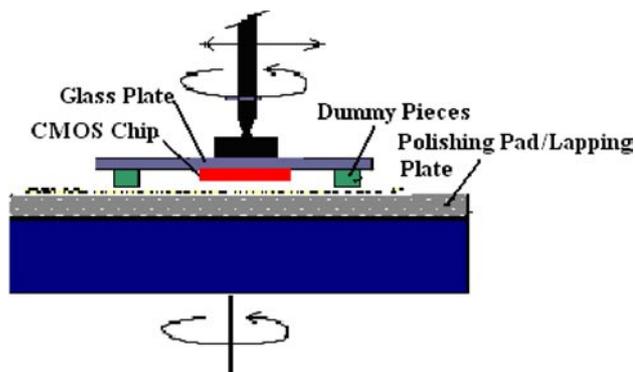
Figure 7. Lapping and polishing configuration.

rotating spindle. The glass plate with chips reciprocates left and right and is free to rotate.

4.2. Formation of a polishing plane

Lapping was used to even out the heights of the dummy pieces and to set a plane for the following polishing process. The lapping abrasive was Al$_2$O$_3$ powder of 3 and 5 μm sizes, and the lapping plate was cast iron. The glass plate thickness was measured at nine locations (eight mounting points for dummy pieces and a center mounting point for the CMOS chip) using a mechanical height gage. The height distribution in figure 8(a) shows that the glass plate has a high and a low region with a difference of 5.5 μm. After attaching the CMOS chip and dummy pieces, their heights were measured (see figure 8(b)). Variation in wax thickness and glass plate thickness causes a height difference between the highest and lowest dummy pieces of 12 μm. After lapping for 20 min with 5 μm slurry followed by 10 min with 3 μm slurry, all pieces were measured again. The CMOS chip was not touched by the lapping plate. The maximum height difference between the dummy pieces after lapping is 5.5 μm, as shown in figure 8(c). This new height distribution is almost consistent with that of the glass plate alone. Given that the diameter of the dummy piece circle is 80 mm, the slope of the dummy piece plane relative to the back of the glass plate is about 0.07 μm mm^{-1}. The difference between the CMOS surface slope and the dummy piece slope causes the subsequent polishing process to produce a tilt error in the CMOS chip surface.

Figure 9 shows dummy chip heights relative to the original CMOS chip height at a number of times during a lapping process. Relative dummy chip heights of 3–24 μm decreased to 2–6 μm after 50 min. Lapping for more than 100 min brought the lapping plate into contact with the CMOS chip surface and caused breakage. This indicates that it is necessary to switch from lapping to polishing before the relative dummy chip heights reach zero.

4.3. Bump removal

Even when the lapping/polishing plane has not yet intersected the CMOS surface, a switch to polishing may produce contact between the pad and the chip surface because the pad is compliant. A height gage was used to measure the deflection of the glass plate (with pieces attached) relative to the lapping
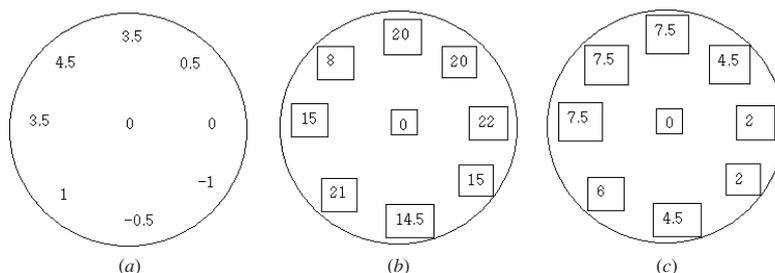
Figure 8. Height measurements (in μm) of glass plate, CMOS chip and dummy pieces: (*a*) glass plate; (*b*) before lapping; (*c*) after lapping.
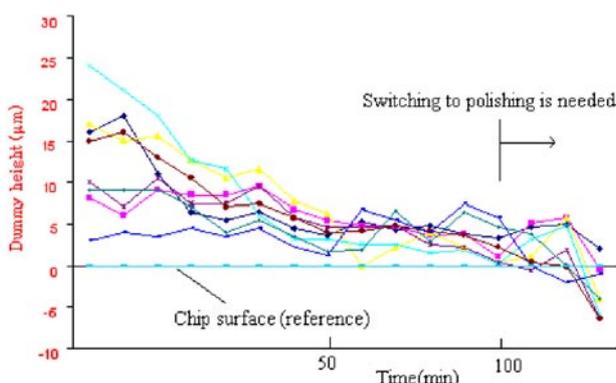
Figure 9. Dummy chip height change during the lapping process.
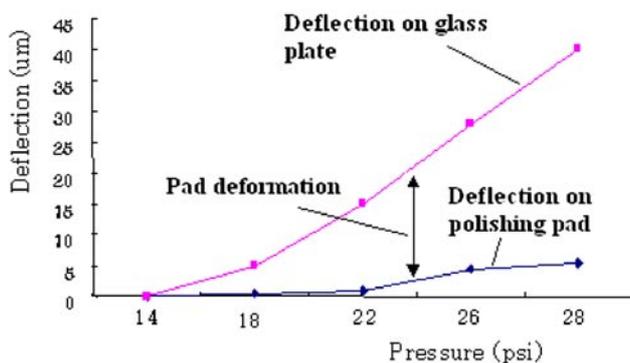
Figure 10. Pad deflection under polishing pressure.
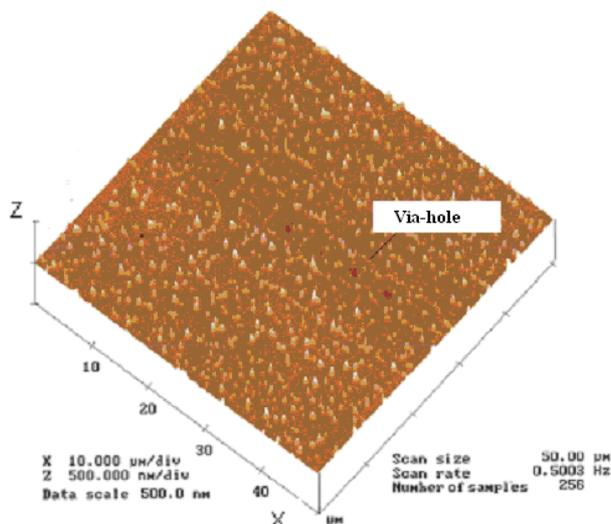
Figure 11. AFM image of the interconnect area after planarization.
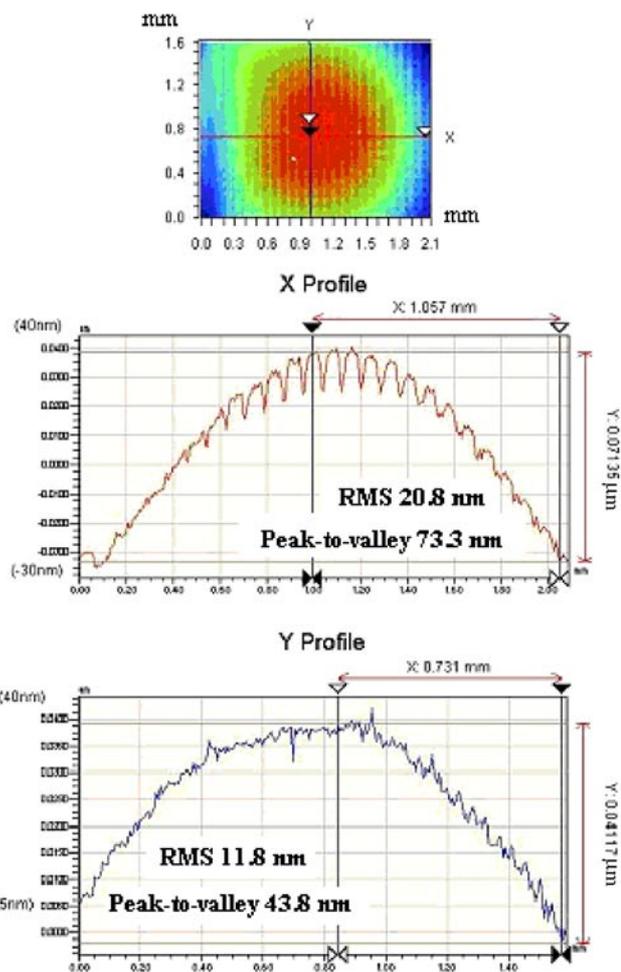
Figure 12. Surface profile of CMOS-1 after planarization.

plate (which carries the polishing pad) as upper platen pressure was applied. Figure 10 shows the deflection of the glass plate and lapping plate for five pressure levels. Subtracting these two deflections yields the pad deformation. This measurement does not include deformation due to the weight of the glass plate carrier. The indicated pressures are those applied by an air cylinder to the upper platen; the deformation amounts are also relative to the pad deformation with the weight of glass carrier resting on top of it. At 28 psi, the net pad deformation is approximately 34.5 μm. This amount of pad deformation indicates that polishing of the CMOS chip can take place even when the dummy pieces are higher than the CMOS surface. Based on this result, we decided to switch from polishing
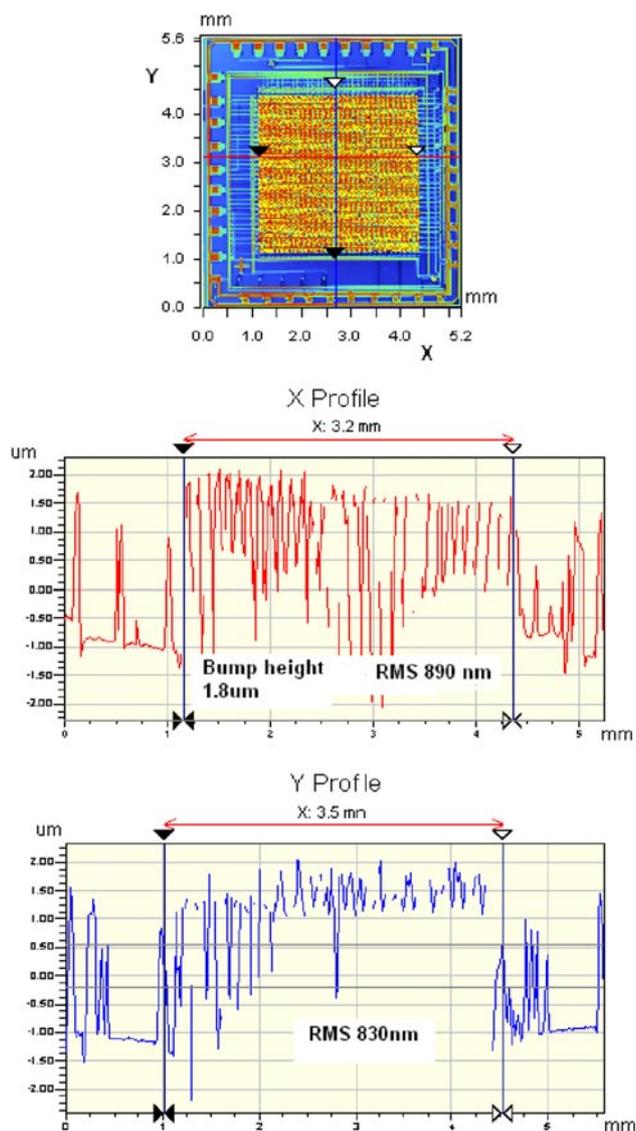
Figure 13. Surface profile of CMOS-2 before planarization.

Figure 14. Height of the four dummy silicon pieces around CMOS-2 after lapping.

to lapping when the dummy piece heights reduced to within 5–10 μm of the CMOS.

The polishing rate for eight silicon dummy pieces was measured when using a colloidal silica slurry, pad spindle speed of 70 rpm, and reciprocating arm spindle speed of 40 rpm. Two air pressures, 20 and 22 psi, were compared for a polishing time of 20 min. For 20 and 22 psi pressure, the polishing rates were 0.13 and 0.23 μm min^{-1}, respectively. The polishing rate depends strongly upon the pressure setting, at least in this range. To compare the polishing rates of silicon and silicon nitride, silicon nitride was deposited on four silicon pieces. These four pieces along with four silicon pieces were placed in an alternating arrangement on the glass plate and were then polished simultaneously until the average height of the silicon pieces was reduced by 4 μm. Measurement of the pieces with silicon nitride surfaces showed that they reduced in height by only 1.25 to 1.5 μm. The polishing rate for the silicon nitride on the CMOS chip should therefore be approximately 1/3 as much as that of the silicon pieces.

A 2.2 μm silicon nitride layer was sputtered onto chips identified as CMOS-1, and dummy pieces were prepared to be 1–7 μm taller than the CMOS chip. After 30 min of polishing, the CMOS surface was measured with an atomic force microscope. The result in figure 11 shows that the bumps and via-holes, which are evident in figure 3, are barely apparent. The residual depth of a hole-like structure is now less than 25 nm, which will be etched in the following via-hole formation.

However, planarization of the chip produced a curvature error. Figure 12 shows the surface profile with curvature error: 73 nm peak-to-valley in the x cross-section and 41 nm peak-to-valley in the y cross-section over a 2 mm length. Tilt error was not included in the measurement.

4.4. Measurement of tilt error

A white light interferometer was used to characterize tilt error after planarization of CMOS-2 chips with initial bumps of 1.8 μm. The initial topography of the chip before polishing was measured, as shown in figure 13. An optical measurement shows the profile of 960 nm root-mean-square (rms) error before planarization.
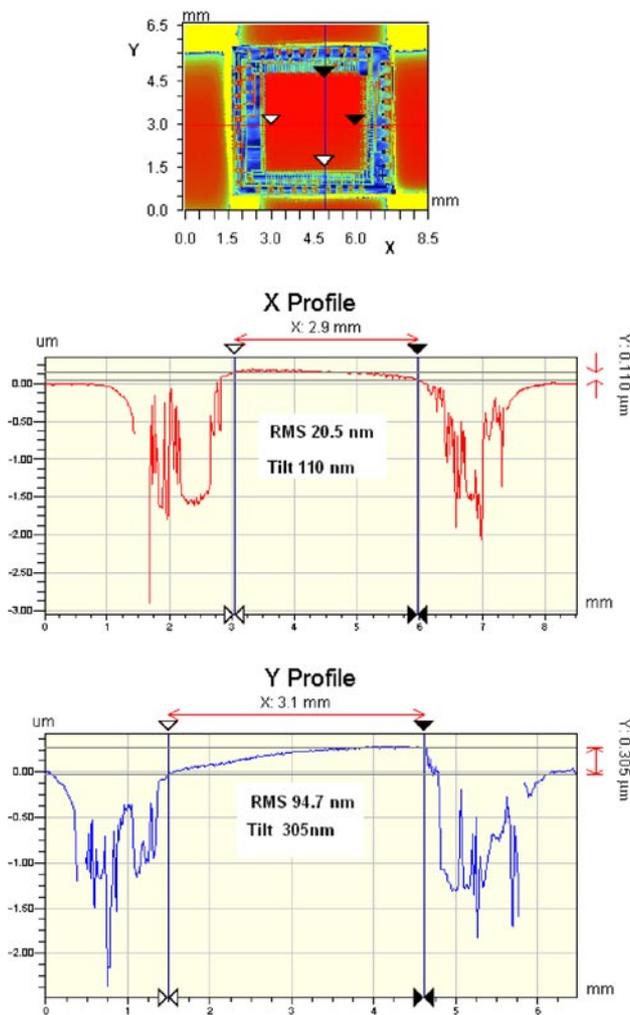
Figure 15. Surface profile of CMOS-2 after planarization.

Silicon nitride of 3 μm was sputtered onto the CMOS chip. For tilt measurement during the planarization process, small four silicon pieces around the chip were added to the glass plate before lapping. After a lapping of the twelve dummy pieces, an optical measurement showed about 10 μm height difference between the dummy and the chip, as shown in figure 14. The field view of the measurement was 8.5 (H) $\times$ 6.4 (V) mm^2. All conditions were the same as that in the previous planarization experiment.

After the subsequent polishing of the lapped chip and dummy pieces, dummy pieces are slightly lower than that of the chip, as shown figure 15. Tilt was 305 nm in the *y*-direction and 110 nm in the *x*-direction from a reference plane consisting of two dummies. This was from the wedge shape of the bonding film. The rms value of the surface flatness was 94.7 nm, mostly from the tilt and the round shape at the edge of the CMOS bumps region. The rms flatness reflects all tilt, curvature error of the chip flatness using two lapped dummy references.

5. Conclusion

In this paper we describe a chip-scale planarization process using low-temperature deposition of silicon nitride and CMP.

The deposition layer is necessary to provide a margin of tilt error for the subsequent polishing process. Deposition temperatures were maintained at low levels to prevent aluminum interconnection damage in the CMOS. The lapping of dummy silicon pieces formed a polishing plane. This process achieved a rms error of 94.7 nm over a 3 mm length including tilt and curvature errors. Neglecting the tilt error, a rms error of 20.8 nm was achieved.

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